Kaparel CompactPCI

Integrated Backplane Architecture Solutions

PS4900/05 Backplane User Manual

PCI INDUSTRIAL PICMG COMPUTERS

PS4900/05 Backplane User Manual

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1 Introduction

The following section will give you a brief overview about your Kaparel product. It will also help you navigate our documentation efficiently.

This chapter will tell you about the following:

- Kaparel Corporation
- Kaparel PS4900/05 backplane
- Contact information
- Document conventions
- Background information

1.1 Kaparel Corporation

Kaparel Corporation develops, manufactures, and globally markets CompactPCI® hardware and software solutions. From our pioneering work in CompactPCI® bridge designs, Kaparel has quickly become a leader in all aspects of CompactPCI® technology. In addition to over 200 “off-the-shelf” standard products, Kaparel designs and produces custom solutions. Specializing in high slot count, hot swap, and high availability systems, Kaparel CompactPCI® solutions are rapidly becoming the choice of major telecommunications and computer manufacturers around the globe.

1.2 Kaparel PS4900/05 backplane

Your PS4900/05 is a 6U x 84HP (21-slot) (16.761 x 10.33”) 10-layer custom backplane designed and manufactured by Kaparel Corporation as part of its standard product offering. The PS4900/05 is one of Kaparel’s PS49XX family of PICMG® 2.16 CPSB backplanes See Section 3 “Quick Start” on page 9 and Section 4 “Understanding Your Backplane”, on page 17 for details.

1.3 Contact information

If you have questions about your new backplane or about Kaparel in general, please contact us by using the following information:

Phone Number: (519) 725-0101

Fax Number: (519) 725-0414

Email Address: support@kaparel.com

Web Address: www.kaparel.com

Mailing Address: Kaparel Corporation
97 Randall Drive
Waterloo, Ontario
Canada N2V 1C5

1.4 Document conventions

You will see the following icons periodically throughout this manual:

The Warning icon cautions you against an action or treatment that could threaten the responsiveness of the Kaparel equipment or the integrity of your current work.

The Note icon notifies you of information that will either make a procedure easier or clarify an earlier description.

1.5 Background information

When you design CompactPCI® systems, use the following documents for reference:

- PICMG® 2.0 Rev 3.0 CompactPCI® Specification as amended by ECN 2.0-3.0-002
- PICMG® 2.1 Rev 2.0 Hot Swap Specification
- PICMG® 2.5 R1.0 Computer Telephony specification
- PICMG® 2.10 R1.0 Keying of CompactPCI® Boards and Backplanes
- PICMG® 2.11 R1.0 Power Interface Specification
- PICMG® 2.16 R1.0 CompactPCI® Packet Switching Backplane
- PICMG® 2.17 R1.0 StarFabric Specification
- PICMG® 2.9 R1.0 System Management specification
- PCI Local Bus Specification Rev 2.2
- PCI Bridge Specification Rev 1.1
- IEEE Std. 1101.1-1998
- IEEE Std. 1101.10-1996
- IEEE Std. 1101.11-1998
- PCI Hardware and Software Architecture & Design 3rd ed. (ISBN 0-929392-32-9)

2 Features

The PS4900/05 backplane has been designed with the following features:

- Two 8-slot 64-bit CompactPCI® buses operating at 33MHz PCI or 66MHz PCI-X.
- Selectable V(I/O) (3.3V or 5V) when configured for 33MHz CompactPCI®.
- PICMG® 2.1 R2.0 compliant Full Hot Swap.
- Provisions for up to four backplane stiffeners to control flex during card insertion.
- PICMG® 2.5 R1.0 compliant H.110 CT buses on all Peripheral Slots (PS4900 only).
- Support for 8HP System Boards at expense of one Peripheral Slot.
- Dual redundant Ethernet interconnect (2 Fabrics + 16 Nodes) as outlined in PICMG® 2.16 R1.0
- Support for Rear Transition Modules in all card slots.
- Configurable power slot support for two 6Ux8HP, three 6Ux4HP, three 3Ux8HP, or four 3Ux4HP supplies.
- All power slots support PICMG® 2.11 R1.0 compatible power supply modules.
- Power input headers for H.110 -Vbat, -SELVbat and VRG power signals.
- ATX power header for auxiliary power input/output .
- Three fan power connectors providing 12V and System Management support.
- Support for Kaparel and I-Bus proprietary alarm cards in slot 17.
- Support for two Kaparel Power Entry Modules (PEMs)
- AC/DC power input header if PEMs are not used.
- PICMG® 2.9 R1.0 compliant System Management Bus (SMBus) support on all slots, power supplies, PEMs, fans, and Alarm Card.
- Support for I^2C bridge function on Alarm Card to support >19 SMBus nodes.

Figure 1 illustrates front and rear system views

Figure 2 and **Figure 3** illustrate the major features of the backplanes, showing approximate locations for all connectors. Objects drawn as solid lines are on the front side of the backplane. Objects drawn as dashed lines are on the rear. Shaded objects are on both sides.

Figure 1: Module Allocation

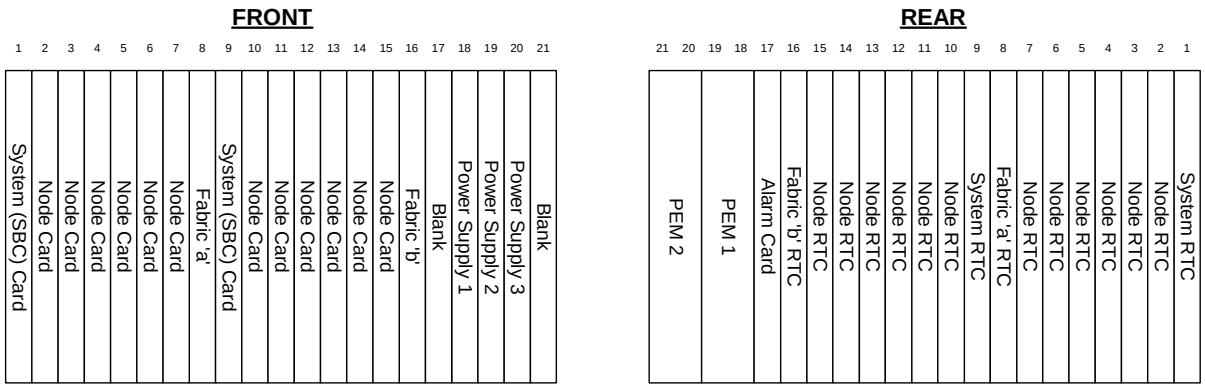


Figure 2: PS4900 Backplane Layout

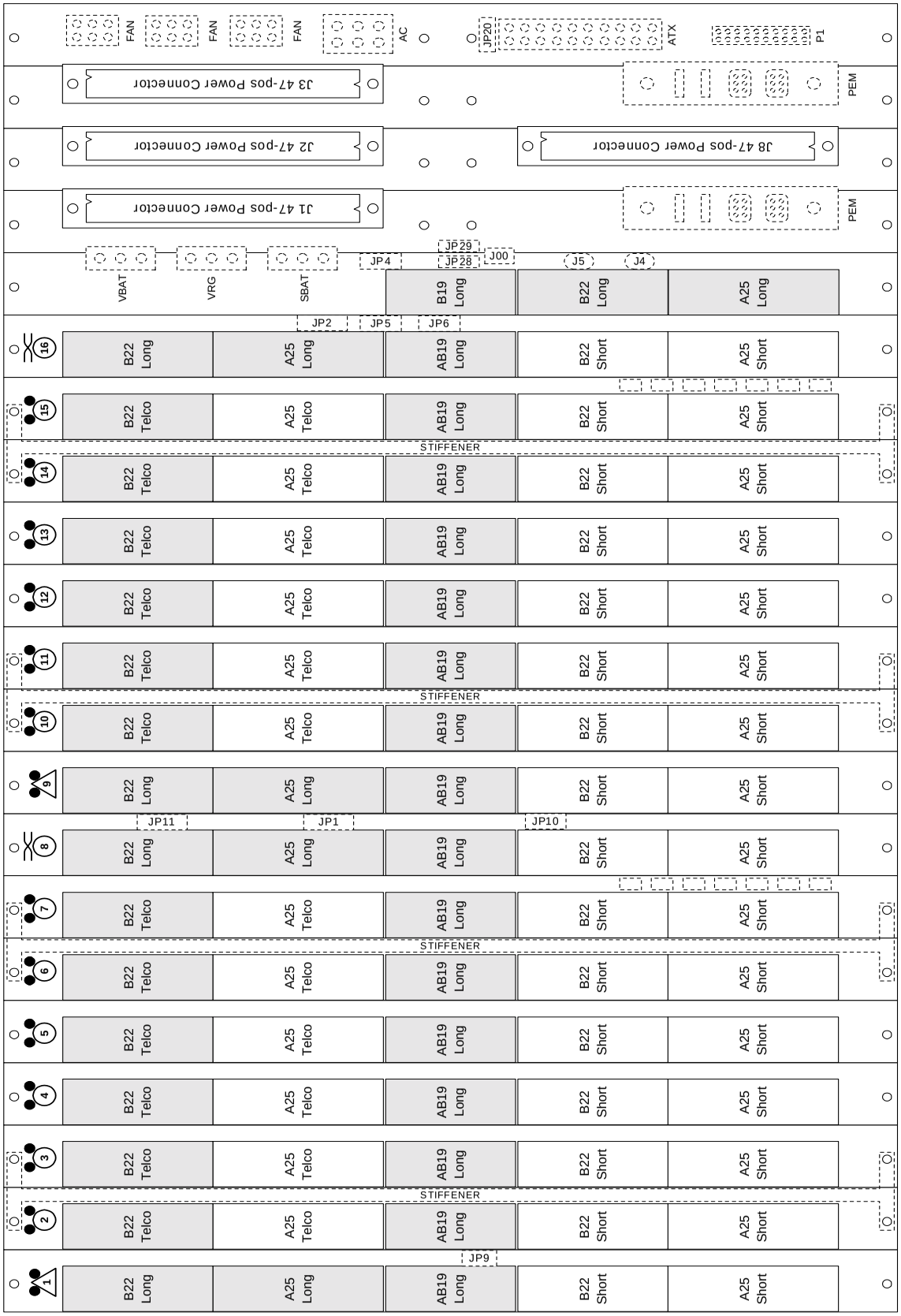
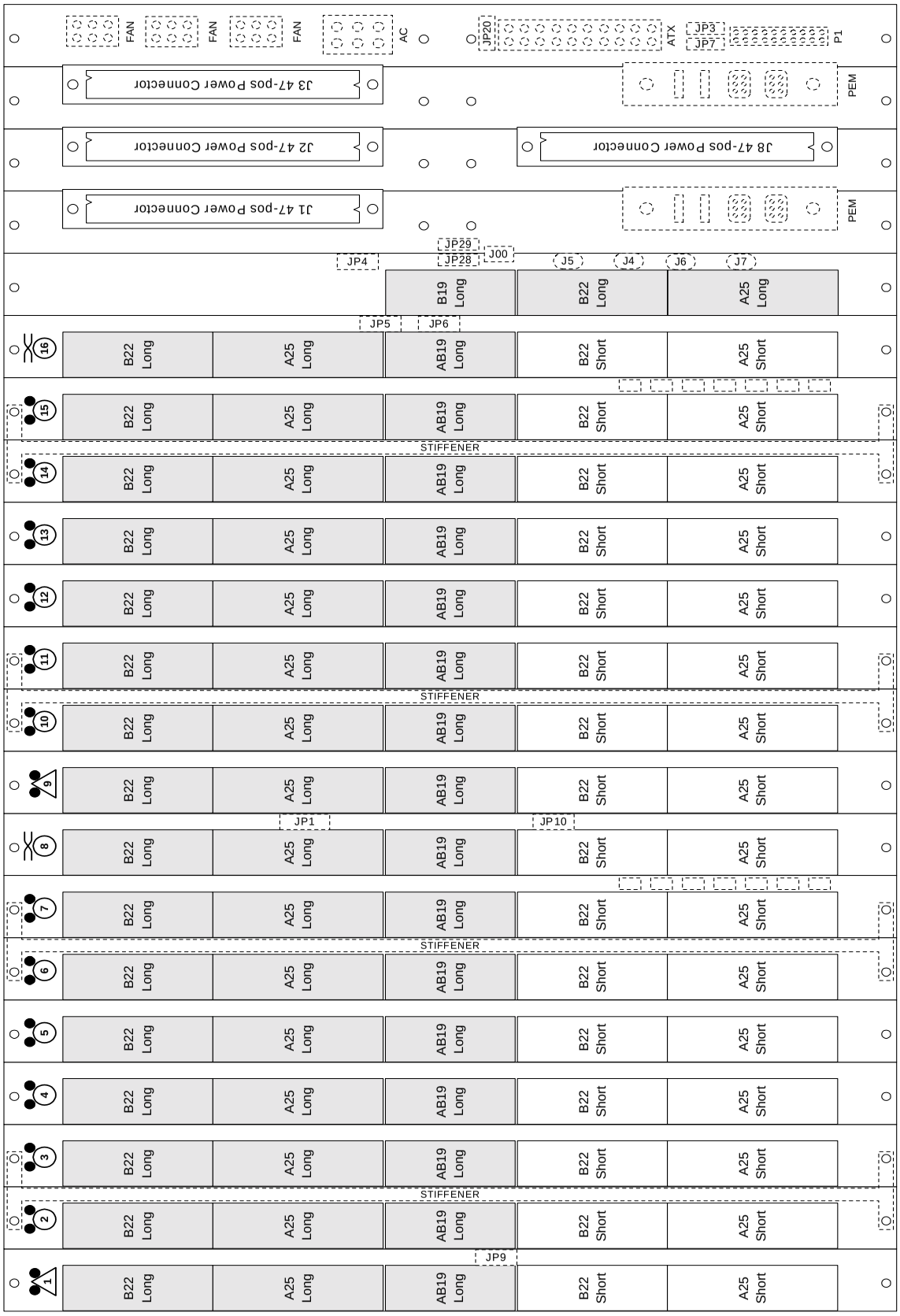


Figure 3: PS4905 Backplane Layout



3 Quick Start

Some older versions of the PS4900/05 will not contain all of the functionality described in this manual. Where ever possible, the areas in question will have an asterisks * highlighting the item in question.

The facilities present on your backplane will depend upon the actual model that you have ordered. Order specific options are highlighted by the dollar $ symbol.

The PS4900/05 backplanes are compliant with the PICMG® 2.0 R3.0 CompactPCI® Core Specification, PICMG® 2. 16 R1.0 CompactPCI® Packet Switching Backplane Specification and the PICMG® 2.5 R1.0 Computer Telephony Specification (PS4900 only), providing a +5V or +3.3V, 33MHz, 64-bit CompactPCI® bus on all P1/P2 connectors and a standard H.110 8Mbps bus on the P4 connectors of slots 2-7 and 10-15 (PS4900 only).

This chapter will provide an overview of basic operating procedures, including the following:

- Inspecting your backplane
- Installing your backplane in a sub-rack
- Powering your backplane
- Accessory connections
- Installing modules in your backplane

3.1 Inspecting your backplane

Take great care when handling the backplane. Improper handling could cause damage to the connector pins.

Always handle the backplane from the edges, never the connectors.

The first item that must be done before starting to utilize your backplane is to perform a thorough inspection.

During the course of handling, shipping and assembly, pins, shrouds, mounting screws and other items could become damaged and/or loose. Operating a damaged backplane could cause serious damage to the backplane and/or devices that interface to it.

Take a few minutes to visually inspect that all of the connector pins are straight, shrouds are properly seated, screws are tight, etc.

Repair any bent pins, shrouds, loose screws, etc. before proceeding. If damage to the backplane is deemed too extensive, call Kaparel Customer Service for assistance on how to proceed.

3.2 Installing your backplane in a sub-rack

The PS4900/05 backplane mounts into a sub-rack using M2.5 screws along the rows of mounting holes situated at the top and bottom end of each slot. Install one screw in each hole and tighten securely. Do not install a screw in the mounting hole(s) marked with digital ground if a connection between chassis (safety) ground and digital (circuit) ground is not

desired. Mounting holes that connects to digital ground are marked with the corresponding symbol (⏚) on the bottom silkscreen. Figure 4 illustrates an example.

If you are installing the optional backplane stiffeners (Kaparel part# 83A100002-A01), you must locate these where shown in **Figure 2** on page 8. The rear side of the backplane will also have silk-screened locators to help in positioning the stiffeners. Figure 4 illustrates the location. Note that the stiffeners are not symmetrical and as such, will only fit properly in one direction. The vertical rib must be centered between the connectors.

Figure 4: Mounting Hole/Stiffener Location

3.3 Powering your backplane

3.3.1 Backplane secondary power

CompactPCI® power for the PS4900/05 backplane is supplied via four (N+1 redundant) 47-pin Positronic connectors located in the right hand section of the backplane. The connectors accept hot-swappable AC/DC power supply units that comply with the PICMG® 2.11 R1.0 specification.

The power supplies accept input as either AC or DC. For more information on the 47-pin Positronic connectors, see Appendix A Section 5.1 on page 32.

3.3.1.1 Power supply configuration

Depending upon your backplane model, you can install up to four power supply modules in the 47-pin power connectors J1, J2($), J3 and J8($). Power supplies are assigned geographic addresses 0 to 3 (J1 – 0, J2 – 1, J3 – 2, J8 – 3), numbering from left to right, when viewed from the front.

Possible configurations are:

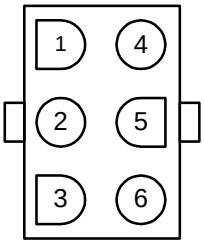
- Two 6Ux8HP supplies
- Three 6Ux4HP supplies
- Four 3Ux4HP supplies
- Three 3Ux8HP supplies

3.3.2 AC/DC power input ($)

One 2x3 style AMP Mate-N-Lok connector (J12) is provided for AC/DC input to the power supplies. The maximum current from line to neutral is approximately 11 Amps (22 Amps total). This figure has been de-rated for a 30C-temperature rise with a minimum cable length of 11.3”. Table 1 displays the connector’s pinout.

Table 1: Pinout of the AC/DC input connector

Pin#	1	4
Signal Name	CH_GND	CH_GND
Pin#	2	5
Signal Name	AC_LINE	AC_LINE
Pin#	3	6
Signal Name	AC_N	AC_N



Alternatively, these terminals can also be used to connect a DC power supply. DC+ and DC- are connected to AC Neutral and AC Line respectively. Please refer to the manufacturer's power supply specifications for exact details.

A clearance of 3.2mm is provided for any AC line on the backlane layers to any secondary circuits on the outside layers, and 1.6mm on inside layers.

If the backplane is equipped with PEM support, connect J12 will not be populated. Connectors J17 and J22 will be populated instead.

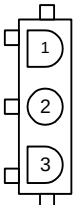
3.3.3 H.110 power (PS4900 only)

The PS4900 provides two H.110 Computer Telephony buses on connector locations P4 and P5 of slots 2-7 and 10-15. All signal nets are isolated between the two CT buses. Telephony power (Vbat, VbatRtn, SELVbat, SELVbatRtn, VRG, and VRGRtn), system power (+5V, +3.3V, +12V, -12V), and all ground nets are common to both bus segments.

Telephony power is connected to the backplane on 1x3 Mate-N-Lok connectors J14, J15 and J16. Mating part is Amp #350766-1. Pinouts for these connectors is shown in **Table 2**.

Table 2: H.110 CT Power Connections

Pin	Connector/Function		
	J14/Vbat	J15/VRG	J16/SELVbat
1	-Vbat	VRG	-SELVbat
2	Chassis Ground	Chassis Ground	Chassis Ground
3	VbatRtn	VRGRtn	SELVbatRtn



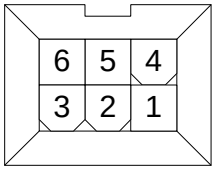
3.4 Accessory connections

3.4.1 Fan control

The PS4900/05 provides three fan connectors, J51, J52 and J53(*), for power and control of 12V DC fans. The connectors provided are 6-position (2x3) Molex Mini-Fit Junior connectors, capable of providing 6A of continuous current (de-rated for 30C temp. rise). Mating connector is Molex #39-01-2060. Figure 5 illustrates the connector outline and pinout for the fan connectors. Note that FAN1 connections are on J51, FAN2 on J52 and FAN3 on J53.

Figure 5: Fan Connectors J51, J52, J53

Description	Pin	Pin	Description
IPMB_PWR	**1**	**4**	FAN[1,2,3]_ALM#
C_IPMB_SCL	**2**	**5**	+12V
C_IPMB_SDA	**3**	**6**	GND



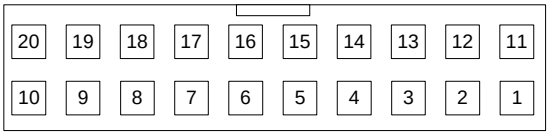
3.4.2 Alarm card I/O

For fans that require PWM, TACH and possibly TEMP control, connector P1 provides signaling for up to 4 of each device.

Table 3 displays the pinout for the connector.

Table 3: I/O Signal Allocation

Description	Pin	Pin	Description
+5V	**1**	**11**	+5V
TEMP1	**2**	**12**	TEMP/1
TEMP2	**3**	**13**	TEMP/2
TEMP3	**4**	**14**	TEMP/3
TEMP4	**5**	**15**	TEMP/4
TACH1	**6**	**16**	PWM1
TACH2	**7**	**17**	PWM2
TACH3	**8**	**18**	PWM3
TACH4	**9**	**19**	PWM4
GND	**10**	**20**	GND



3.4.3 Power Entry Module support ($)

Each PS4900/05 backplane can optionally support two Kaparel Power Entry Modules (PEMs) in the rear of slots 18 and 20. These modules can be utilized used to provide filtered –48V DC or AC input power to the backplane power supplies.

Each PEM connector is capable of supplying 35A when fully derated.

The PEM connectors support Geographic Addressing. Connector J22 is assigned address 5 and J17, address 6.

The power and status signals used by the PEMs is shown in Figure 6 and Table 4.

Figure 6: PEM Connector (Backplane Rear View)

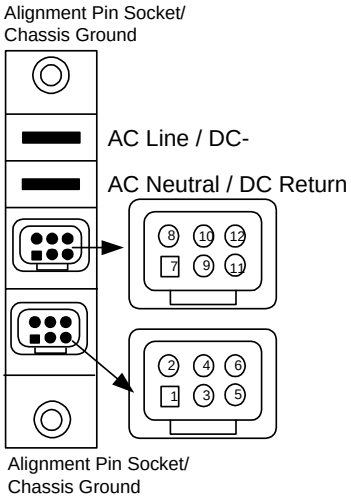


Table 4: PEM Pinout

Pin #	Signal Name	Description
1	PEM#_INH	Alarm Card signal to the PEM to turn the output power on or off.
2	PEM#OUTOK	Signal from the PEM to the Alarm Card indicating PEM output power status.
3	PEM#INOK	Signal from the PEM to the Alarm Card indicating PEM input power status.
4	GND	PEM fully inserted enabling the PEM power output.
5	PEM#_PR	'PEM present' signal to the Alarm Card.
6	GND	Digital ground.
7	C_IPMB_SCL	System management data clock.
8	C_IPMB_SDA	System management data.
9	IMPB_PWR	System management power.
10	GA0	Geographic address bit 0.
11	GA1	Geographic address bit 1.
12	GA2	Geographic address bit 2.

If the backplane is not equipped with PEM support, connector J17 and J22 will not be populated. Connector J12 will be populated instead.

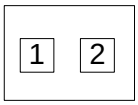
3.4.4 Miscellaneous headers

3.4.4.1 External reset

The push button reset of the Host Slots are connected to individual 2-pin headers (JP9 and JP10). These connectors allow for external reset switches (or switch) to be connected to the Host Slots. JP9 is connected to Host Slot 1. JP10 is connected to Host Slot 9. Table 5 displays the pinout of the connectors.

Table 5: Reset Connectors

Pin#	Signal Name
1	GND
2	PRST#



3.4.4.2 Power status and control

The PS4900/05 routes all DEG#, FAL# and INH# signals as shown in Figure 7. Three headers (JP4, JP5, and JP6) are provided for Or'ing and routing of the DEG# and FAL# signals to the system slots. The INH# signals route to J100.

Figure 7: Power Status and Control Signal Routing

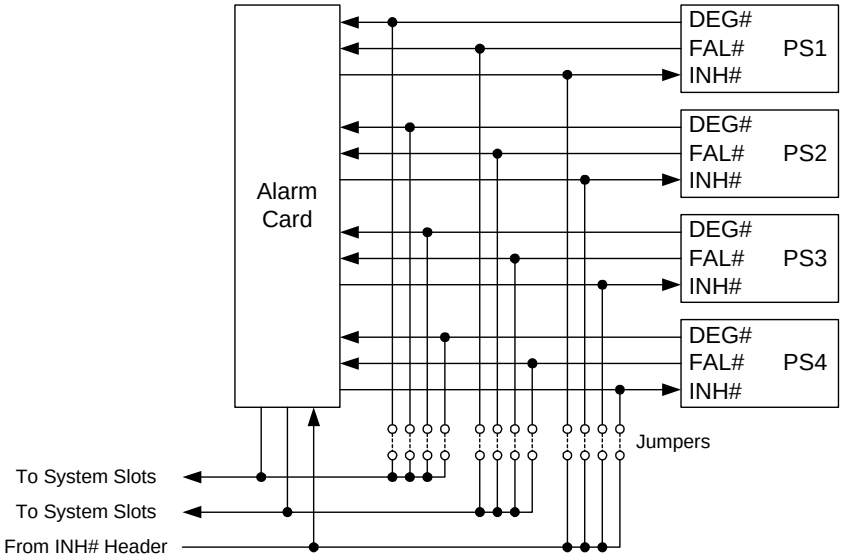


Table 6, Table 7 and Table 8 display the configuration of the power supply configuration headers.

Table 6: INH# Header

Description	Pin	Pin	Description
INH#	1	2	INH1#
INH#	3	4	INH2#
INH#	5	6	INH3#
INH#	7	8	INH4#

Table 7: FALN Header

Description	Pin	Pin	Description
FALN	1	2	FAL1N
FALN	3	4	FAL2N
FALN	5	6	FAL3N
FALN	7	8	FAL4N

Table 8: DEGN Header

Description	Pin	Pin	Description
DEGN	1	2	DEG1N
DEGN	3	4	DEG2N
DEGN	5	6	DEG3N
DEGN	7	8	DEG4N

If the SBCs support the INH#, DEGN and FALN signals and there is no Alarm Card in slot 17, these shunts should be populated.

If the Alarm Card is populated in slot 17, these shunts **must be** removed.

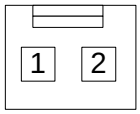
3.4.4.3 Power supply inhibit

J100 can be wired to a switch on the chassis which can be utilized in “Inhibiting” the secondary power. This will not turn off the power supplies but only their output voltages. When using a PC ATX power supply, the header should be shorted to turn the power supply outputs “ON”.

Table 9 displays the pinout of the connector.

Table 9: Power Supply Inhibit Connector

Pin#	Signal Name
1	INH#
2	GND



3.5 Installing modules in your backplane

The PS4900/05 supports up to 16 add-in CompactPCI®/H.110 cards and four power supplies. Slots are numbered 1 through 16 from left to right as viewed from the front of the sub-rack. For more information on slot locations, see **Figure 2** on page 8. For more information on module allocation, see **Figure 1** on page 7.

Do not use excessive force when installing or removing modules from the chassis. Use of excessive force can result in damage to the backplane and/or module.

Should excessive force be required, remove the module(s) and verify the alignment of the mechanicals and backplane.

There is no preset order to inserting modules into the backplane. Refer to the module and/or chassis User Manual(s) for more information on inserting modules.

The Host slots (1 and 9) are configured for SBCs that support 2.16 Ethernet connections. Inserting non-2.16 SBC into these slots may cause damage to the SBCs and/or Fabric Boards.

4 Understanding Your Backplane

The backplane provides for sixteen (16) single width plug-in board slots on a 0.8” pitch and four (4) single width power supply slots. There are two System Slots and fourteen Peripheral Slots. The PS4900/05 is not designed for use with the PS1134 and PS1133 Kaparel low profile CompactPCI® bridges or the PS1130 Kaparel Pallet (i.e. it can be used only as a standalone unit).

4.1 Backplane connectors

The complete list of connectors utilized on the backplane is listed in Backplane connectors Table 26 on page 33.

4.1.1 Power connectors

The PS4900/05 backplane distributes DC power (+5V, +3.3V, +12V & -12V) to each slot through the internal 1oz. copper planes which connect to the 47-pin Positronic connectors (J1, J2, J3 and J8). The AC/DC input to the power supplies is provided by internal traces routed to support up to **8A** current carrying capability from J12 or optionally from J17 and J22. The part numbers and reference designators for the power connectors are listed in Table 26 on page 33.

The output provided by the optional PEMs is common to all power supplies.

The output provided by the power supplies is common to all of the CompactPCI® slots. The power supply units are connected in load sharing mode. The large contacts (size 16) have a current capacity of 40A each, derated to 23A for a 30ºC temperature rise. The small contacts (size 20) have a capacity of 28A each, derated to 16.5A for a 30ºC temperature rise. The connector pinout assignments and mechanical location for power supplies is according to the PICMG® 2.11 R1.0 Power Interface Specification.

Remote voltage sensing for the CompactPCI® power rails is employed by default on the PS4900/05 backplane.

4.2 V(I/O) power

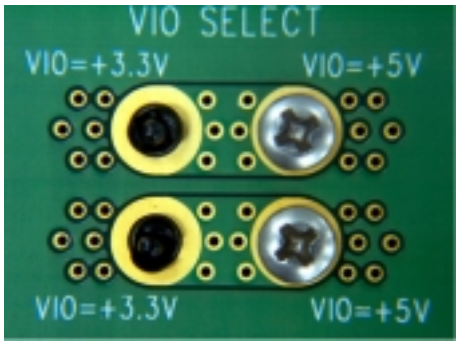
Configuration of the V(I/O) is factory defaulted depending upon customer request by shorting the V(I/O) internal plane on the PCB to either the +5V or +3.3V plane. The selection is realized by mounting standard stainless steel M2.5 screws in the corresponding holes marked for the corresponding voltage. **Figure 8** illustrates a typical V(I/O) selection mechanism.

The V(I/O) configuration is checked against the keying on the P1 backplane connector at the time of assembly and test at the factory. The keying mechanism on P1 is used to prevent a board built with one buffer technology (+3.3V or +5V) from being inserted into a system designed for the other buffer technology (+5V or +3.3V respectively).

Please note that a 66 MHz platform should always be configured for +3.3V operation on the V(I/O), according to the PICMG® 2.0 R3.0 CompactPCI® Core Specification.

The selectable V(I/O) feature is <u>not</u> intended to be field upgradeable. Therefore the V(I/O) screws <u>must be left in the factory default positions</u> and the board returned to the factory if switching to a different V(I/O) is necessary. Kaparel does not assume responsibility for changes of the V(I/O) configuration of the backplane not made and tested at the factory.

Figure 8: V(I/O) Selection



4.3 Slot keying

The P1 and P4 on the backplane are keyed in accordance with the PICMG® 2.10 R1.0 specification.

Backplanes configured for 3.3V V(I/O) have P1 on all slots keyed with the “cadmium yellow” RAL #1021 Code 1278 key.

Backplanes configured for 5V V(I/O) have P1 on all slots keyed with the “brilliant blue” RAL #5007 Code 2348 key.

P4 on slots 8 and 16 are keyed with the “blue/lilac” RAL #4005 Code 2478 key which signifies that they are configured as Standard 2.16 Fabric slots.

P4 on slots 1 and 9 are keyed with the “nut brown” RAL #8011 Code 4578 key which signifies that P4 is for user I/O.

On the PS4900, P4 on slots 2 to 7 and 10 to 15 are keyed with the “strawberry red” RAL #3018 Code 3567 key which signifies that P4 is configured for H.110. On the PS4905, the P4 connectors are keyed with the “nut brown” RAL #8011 Code 4578 key which signifies that P4 is for user I/O.

Keys on the modules must be inserted and set according to the above. Failure to do so could result in damage to the backplane and/or modules.

4.4 Buses on the backplane

4.4.1 CompactPCI® bus

The PS4900/05 has 2 eight-slot segments that provide +5V or +3.3V, 33MHz, 64-bit CompactPCI® buses on the P1-P2 sections. All aspects of the buses meet the PICMG® 2.0 R3.0 CompactPCI® Core Specification. The backplane also complies with the PICMG® 2.1 R1.0 Hot Swap Specification.

The first segment begins in slot 1 and extends to slot 8. The segment is Hosted in slot 1 and can accept a single slot wide (4HP) SBC. The second segment, begins in slot 9 and extends to slot 16. This segment is Hosted in slot 9 and also accepts a single slot wide SBC.

Signal M66EN is connected directly to GND to force 33MHz operation.

Signal 64EN is connected directly to GND to enable 64-bit transfers.

The pinouts for the P1/P2 CompactPCI® section are shown Appendix B **Table 27** and **Table 28**. The PS4900/05 backplane uses 2mm male short tail connectors for the P1/P2 area. The P1 connectors are A25 HotSwap and the P2 connectors are B22.

Clock lines are supplied from the Host slots and are routed in conformance to the PICMG® 2.0 R3.0 specification. Each Peripheral slot gets an individual clock line from its System Slot. The skew between different clock lines is minimized by matching the traces in length (6.5") and routing them on the same internal layer.

The PS4900/05 can act only as a stand-alone backplane. The backplane is not designed to support the PS1132 (64-bit) or PS1131 (32-bit) low profile Kaparel CompactPCI® bridges. The PS4900/05 also does not support the PS1130 Kaparel Pallet Bridge.

4.4.1.1 Decoupling

Power decoupling for the CompactPCI® bus meets all Rev 3.0 CompactPCI® specification requirements, providing 47µF of capacitance per slot for each of the +5V and +3.3V voltage rails in the P1/P2 area between slots, 94µF of capacitance for the V(I/O) voltage rail and 15µF capacitance for each of the +12V and –12V rails. Additionally, 100nF ceramic capacitors are provided at each slot.

4.4.1.2 Slot identification

A 5-bit physical slot number is used for the purpose of uniquely identifying each slot on the PS4900/05 backplane. The geographic address is in a simple binary count format. On the backplane, the address is encoded by grounding or leaving unconnected different combinations of pins at each slot connector. **Table 10** displays the physical slot number, its geographic address and the corresponding P2 pin settings. Physical slot "0" is not used as numbering starts with "1'.

Please note that the geographic address of each CompactPCI® slot and each of the power supply slots is hardwired on the backplane. This is not to be confused with the shelf address of the system (if equipped).

Table 10: Slot Address Settings

Physical Slot Number	Geographic Address	GA(4) Pin 1, 2 P2-A22	GA(3) Pin 3, 4 P2-B22	GA(2) Pin 5, 6 P2-C22	GA(1) Pin 7, 8 P2-D22	GA(0) Pin 9, 10 P2-E22
1	1	Shorted	Shorted	Shorted	Shorted	Open
2	2	Shorted	Shorted	Shorted	Open	Shorted
3	3	Shorted	Shorted	Shorted	Open	Open
4	4	Shorted	Shorted	Open	Shorted	Shorted
5	5	Shorted	Shorted	Open	Shorted	Open
6	6	Shorted	Shorted	Open	Open	Shorted
7	7	Shorted	Shorted	Open	Open	Open
8	8	Shorted	Open	Shorted	Shorted	Shorted
9	9	Shorted	Open	Shorted	Shorted	Open
10	10	Shorted	Open	Shorted	Open	Shorted
11	11	Shorted	Open	Shorted	Open	Open
12	12	Shorted	Open	Open	Shorted	Shorted
13	13	Shorted	Open	Open	Shorted	Open
14	14	Shorted	Open	Open	Open	Shorted
15	15	Shorted	Open	Open	Open	Open
16	16	Open	Shorted	Shorted	Shorted	Shorted

The power supplies also support geographic addressing. Table 11 displays the allocation of addresses on the power supplies.

Table 11: Power Supply GA

1	2	3
	4	

Geographic addressing is not configurable on the PS4900/05 backplane.

4.4.1.3 PCI-X support

The PS4900/05 backplanes are designed to support future compatibility with PCI-X signaling at 66MHz clock rates. By default, all backplanes are configured for 33MHz PCI operation only. For more information about PCI-X capabilities, please contact Kaparel technical support.

4.4.1.4 Resource allocation

Table 12 displays the allocation of resources on the CompactPCI® buses.

Table 12: Resource Allocation

Phys Slot	Slot Description	Logic Slot	Bus Wdt	IDSEL Map	REQ/GNT Map	PCI CLK Map	Interrupt				Geogr Addr.
							A	B	C	D	
1	HPB	1	64	-	-	-	A	B	C	D	00001
2	PPB	2		PAD31	PREQ/PGNT0	PCLK5	D	A	B	C	00010
3	PPB	3		PAD30	PREQ/PGNT1	PCLK6	C	D	A	B	00011
4	PPB	4		PAD29	PREQ/PGNT2	PCLK1	B	C	D	A	00100
5	PPB	5		PAD28	PREQ/PGNT3	PCLK2	A	B	C	D	00101
6	PPB	6		PAD27	PREQ/PGNT4	PCLK3	D	A	B	C	00110
7	PPB	7		PAD26	PREQ/PGNT5	PCLK4	C	D	A	B	00111
8	PPB	8	64	PAD25	PREQ/PGNT6	PCLK0	B	C	D	A	01000
9	HSB	1	64	-	-	-	A	B	C	D	01001
10	PSB	2		SAD31	SREQ/SGNT0	SCLK0	D	A	B	C	01010
11	PSB	3		SAD30	SREQ/SGNT1	SCLK6	C	D	A	B	01011
12	PSB	4		SAD29	SREQ/SGNT2	SCLK2	B	C	D	A	01100
13	PSB	5		SAD28	SREQ/SGNT3	SCLK4	A	B	C	D	01101
14	PSB	6		SAD27	SREQ/SGNT4	SCLK1	D	A	B	C	01110
15	PSB	7		SAD26	SREQ/SGNT5	SCLK5	C	D	A	B	01111
15	PSB	8	64	SAD25	SREQ/SGNT4	SCLK0	B	C	D	A	10000

PPB = Peripheral on Primary Bus HPB = Host on Primary Bus

PSB = Peripheral on Secondary Bus HSB = Host on Secondary Bus

4.4.2 Segment type identification

The PS4900/05 supports segment type identification as per the PICMG® 2.0 R3.0 ECN 2.0-3.0-002. The backplane is configured for Nominal Right.

Table 13 displays the pin setting for identification .

Table 13: Identification Pin Settings

Segment Type Name	ST[1] (P2-D21)	ST[0] (P2-E21)
Reserved	GND	GND
Nominal Left	GND	Open
Nominal Right	Open	GND
Unknown	Open	Open

4.4.3 CompactPCI® Ethernet fabric

The PS4900/05 backplane supports an Ethernet-based switch fabric interconnect based on the PICMG® 2.16 R1.0 CompactPCI® Packet Switched Backplane specification. The PS4900/05 has support for two Standard Fabric Boards and fourteen Dual-Link Node Boards. All Links are capable of 10, 100, or 1000 Mbps Ethernet signaling.

4.4.3.1 Fabric Slots

Slots 8 and 16 on the PS4900/05 are Fabric Slots. Slot 8 is designated as Fabric 'a' and slot 16 is Fabric 'b'. Standard Fabric Boards supporting up to 20 Links (19 Node Links and one Fabric-to-Fabric Link) can be inserted, although only 14 Links (1-14) are routed to Node Slots on the backplane. The Fabric-to-Fabric Link is also supported. The remaining Node Links (15-19) **may** be used on a rear transition module, as long as all requirements of the PICMG® 2.16 specification are met.

The Fabric Slots support CompactPCI® peripheral connections on P1 and P2. Fabric Slot P3, P4, and P5 connectors are defined for Link connections and BP(I/O) as per the PICMG® 2.16 specification.

Table 30 on page 38 displays the pin assignments for Standard Fabric Slots.

4.4.3.2 Node Slots

Slots 1-7 and 9-15 on the PS4900/05 are Dual Link Node Slots. As such, all Node Slots support links to Fabrics 'a' and 'b'. Node Slots are designated as Nodes 1-14 starting with the lowest numbered slot. Table 14 displays the physical slot to Node mapping.

Table 14: Node Slot Mapping

Slot	Node	Link		Slot	Node	Link
1	1	1		**9**	8	8
2	2	2		**10**	9	9
3	3	3		**11**	10	10
4	4	4		**12**	11	11
5	5	5		**13**	12	12
6	6	6		**14**	13	13
7	7	7		**15**	14	14
8	-	-		**17**	-	15

Node Slots 1 and 9 are System Slots for the two CompactPCI® segments on the PS4900/05

Node Slots 2-7 and 10-15 also support 64-bit/33MHz CompactPCI® peripheral connections on P1 and P2. P3 is used for Link connections and BP(I/O) as per the PICMG® 2.16 specification.

4.4.3.3 Shelf address headers

To comply with the 2.16 CompactPCI® Packet Switching Backplane specification, there are two sets of 5 jumpers (denoted JP1 and JP2 in **Figure 2**) that set the geographic address of the Fabric Slots (Refer to Table 16 for the shelf address settings).

The user can define the address of the Fabric Slots by mounting shunts on headers JP1 and JP2. Table 16 displays the pinout of the headers while Table 17 displays possible settings for these jumpers.

Table 15: Shelf Address Headers

Pin Number	Net name	Pin Number	Net name
1	GND	**2**	FAB_[A,B]_SGA4
3	GND	**4**	FAB_[A,B]_SGA3
5	GND	**6**	FAB_[A,B]_SGA2
7	GND	**8**	FAB_[A,B]_SGA1
9	GND	**10**	FAB_[A,B]_SGA0

Table 16: Fabric Address Configuration

Shelf	Pin 1, 2	Pin 3, 4	Pin 5, 6	Pin 7, 8	Pin 9, 10
1	Shorted	Shorted	Shorted	Shorted	Open
2	Shorted	Shorted	Shorted	Open	Shorted
3	Shorted	Shorted	Shorted	Open	Open
4	Shorted	Shorted	Open	Shorted	Shorted
5	Shorted	Shorted	Open	Shorted	Open
6	Shorted	Shorted	Open	Open	Shorted
7	Shorted	Shorted	Open	Open	Open
8	Shorted	Open	Shorted	Shorted	Shorted
9	Shorted	Open	Shorted	Shorted	Open
10	Shorted	Open	Shorted	Open	Shorted
11	Shorted	Open	Shorted	Open	Open
12	Shorted	Open	Open	Shorted	Shorted
13	Shorted	Open	Open	Shorted	Open
14	Shorted	Open	Open	Open	Shorted
15	Shorted	Open	Open	Open	Open
16	Open	Shorted	Shorted	Shorted	Shorted
17	Open	Shorted	Shorted	Shorted	Open
18	Open	Shorted	Shorted	Open	Shorted
19	Open	Shorted	Shorted	Open	Open
21	Open	Shorted	Open	Shorted	Open

For proper system operation, it is essential that the two jumper headers be set to the same geographic address.

If the backplane is equipped with an H.110 bus then these jumpers must be set to the H.110 shelf address.

4.4.4 H.110 bus (PS4900 only)

4.4.4.1 H.110 pinout

The PS4900 supports the H.110 Computer Telephony Bus on the P4 connector of slots 2 through 7 and 10 through 15 in conformance with the PICMG® 2.5 R1.0 Computer Telephony Specification (please refer to Appendix B Table 29 for details on pinout). The H.110 bus is not routed to the System Slots. This has been done to enable the use of SBCs cards that require the P4 connector for front and rear I/O. Passive terminations are

provided at both ends of the H.110 bus for the signals CT_C8_A, CT_C8_B, CT_FRAME_A#, CT_FRAME_B#.

In addition to this, the P5 area is reserved for H.110 related user I/O. This section is loaded with long tail transition connectors with shrouds on the rear side of the backplane to allow interfacing with rear cards. None of the pins on the P5 area are bussed on backplane except for the row F ground and chassis ground pins.

4.4.4.2 Decoupling

Power decoupling for the H.110 bus is provided by one 47µF tantalum capacitor per slot for each of the +5V and +3.3V voltage rails in the P4 area between slots and 15µF tantalum capacitors for each of the +12V and –12V rails. Additionally, 100nF ceramic capacitors are provided at each slot.

4.4.4.3 H.110 reset control

Two resistors (R107 and R14) are included to allow for the segmentation of the H.110 reset lines from the PRST# signal on their corresponding segment. By default, these resistors are populated thereby connecting the H.110 resets to their corresponding CompactPCI® PRST# signal. R107 controls the H.110 reset on the first H.110 segment (slots 2-7) and R14 controls the second.

4.4.4.4 Shelf address header

Because the PS4900 can be a part of a multi-shelf CompactPCI® system, there is one set of 5 jumpers (denoted JP11 in **Figure 2** on page 8) that set the shelf enumeration address of the backplane (Refer to Table 18 for the shelf address settings).

The user can define the shelf address of the system by mounting shunts on jumper header JP11. **Table 17** displays the pinout of the shelf address header while Table 18 displays possible settings for these jumpers.

Table 17: Shelf Address Header

Pin Number	Net name	Pin Number	Net name
1	GND	**2**	SGA4
3	GND	**4**	SGA3
5	GND	**6**	SGA2
7	GND	**8**	SGA1
9	GND	**10**	SGA0

Table 18: Shelf Address Configuration

Shelf Address	Pin 1, 2	Pin 3, 4	Pin 5, 6	Pin 7, 8	Pin 9, 10
1	Shorted	Shorted	Shorted	Shorted	Open
2	Shorted	Shorted	Shorted	Open	Shorted
3	Shorted	Shorted	Shorted	Open	Open
4	Shorted	Shorted	Open	Shorted	Shorted
5	Shorted	Shorted	Open	Shorted	Open
6	Shorted	Shorted	Open	Open	Shorted
7	Shorted	Shorted	Open	Open	Open
8	Shorted	Open	Shorted	Shorted	Shorted
9	Shorted	Open	Shorted	Shorted	Open
10	Shorted	Open	Shorted	Open	Shorted
11	Shorted	Open	Shorted	Open	Open
12	Shorted	Open	Open	Shorted	Shorted
13	Shorted	Open	Open	Shorted	Open
14	Shorted	Open	Open	Open	Shorted
15	Shorted	Open	Open	Open	Open
16	Open	Shorted	Shorted	Shorted	Shorted
17	Open	Shorted	Shorted	Shorted	Open
18	Open	Shorted	Shorted	Open	Shorted
19	Open	Shorted	Shorted	Open	Open
21	Open	Shorted	Open	Shorted	Open

4.4.5 System management buses

The PS4900/05 backplane routes two System Management Buses as defined in the PICMG® 2.9 R1.0 specification and a third system level bus.

The backplane supports system management on all slots, power supplies, PEMs, fans and alarm card. The bus supports several configuration options:

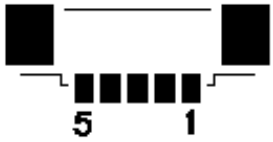
- Two independent IPMB Baseboard Management Controllers (BMCs) in slots 1 and 9
- BMC in Host slot 1 controlling all other slots and devices
- BMC in the alarm card slot (slot 17) controlling all slots and devices

The standard connector for PICMG® System Management off-board extension is the Molex 1.25mm pitch, Micro Wire-to-Board and Wire-to-Wire series or mateable equivalent in a five-pin configuration. The reference receptacle for the System Management extension headers is Molex part number 51021-0500 or equivalent.

Table 19 displays the description of the connector used for the buses and their pinout.

Table 19: Molex connector used for SMB and its pinout

Pin	J4	J5
1	A_IPMB_SCL	B_IPMB_SCL
2	GND	GND
3	A_IPMB_SDA	B_IPMB_SDA
4	IPMB_PWR	IPMB_PWR
5	A_SMB_ALERT#	B_SMB_ALERT#



As an I^2C based bus, the SMBus is restricted by electrical loading limits to 19 devices (nodes). This limitation can be overcome by using I^2C bridge devices to connect bus segments into a single logical bus. Bridge devices may be used on the alarm card (slot 17) to allow all slots and accessory devices to be connected by a single SMBus. This feature will be configurable on the alarm card by the system developer.

IPMB0 (J4) connects to all backplane slots in the first segment (slots 1-8) and the Alarm Card. It consists of IPMB_PWR (pin A4 on P1 of all slots), A_IPMB_SCL (pin B17) and A_IPMB_SDA (pin C17).

IPMB1 (J5) connects to all backplane slots in the second segment (slots 9-16) and to the Alarm Card. IPMB1 consists of IPMB_PWR (pin A4 on P1), B_IPMB_SCL (pin D19 on P2) and B_IPMB_SDA (pin C19 on P2) and B_SMB_ALERT# (pin E19 on P2).

Table 20 displays the allocation of resources on the IPMB buses.

Table 20: IPMB Allocation

Slot / Device	Bus A IPMB0	Bus A IPMB1	Bus B IPMB0	Bus B IPMB1	Accessory SMbus
Slot 1	●	●			
Slot 2	●				
Slot 3	●				
Slot 4	●				
Slot 5	●				
Slot 6	●				
Slot 7	●				
Slot 8	●				
Slot 9			●	●	
Slot 10			●		
Slot 11			●		
Slot 12			●		
Slot 13			●		
Slot 14			●		
Slot 15			●		
Slot 16			●		
Alarm Card	●		●		●
Ext Conn J4	●				
Ext Conn J5			●		
Ext Conn J6*				●	
Ext Conn J7*		●			

Slot / Device	Bus A IPMB0	Bus A IPMB1	Bus B IPMB0	Bus B IPMB1	Accessory SMbus
PS 1					●
PS 2					●
PS 3					●
PS 4					●
PEM 1					●
PEM 2					●
Fan 1					●
Fan 2					●

The IPMB_PWR line can be shorted to +5V through the jumpers JP28, JP29, JP3* and JP7* in case a battery backup does not exist within the chassis for System Management functions.

* denotes PS4905 only

The third System Management Bus is routed from the Alarm Card connector to the IPMB capable accessories.

Sites for pull-up resistors on the IPMB_SCL and IPMB_SDA lines are provided on the backplane for each of the 4 groups of signals. These are populated with a value that will be determined after integration since it is dependent on the value of the total capacitance on the IPMB_SCL and IPMB_SDA lines. The resistors are needed for the line loading on the IPMB bus introduced by each node on the IPMB bus. The biasing of the lines must be kept between 700ns and 1400ns.

4.5 Alarm card (slot 17)

Slot 17 supports an Alarm Card. The slot is designed to support a rear mounted PS6700 or I-Bus Alarm Card and a front mounted PS6701. The PS4900/05 provides connectors in CompactPCI® defined connector positions P1, P2 and P3 (P1 and P2 front and rear).

The alarm slot supports (PS670x only) five SMBus connections, as described in Section 4.4.5. The Alarm Card functionality with regard to SMBus connections is not yet defined, but may be used to bridge all SMBus segments together into one functional bus. The Alarm Card may also contain the SMBus Baseboard Management Controller.

The PS4900/05 alarm slot also connects to individual power supply DEG#, FAL# ,and INH# signals, to allow the Alarm Card to monitor and control up to four power supplies.

PEM status and control signals are routed to the Alarm slot connectors, as described in Section 3.4.4.2 on page 15.

Table 21 and Table 22 show pin assignments for the Alarm Slot.

Table 21: Pinout for Alarm Slot P3

		Column						
	Row	Z	A	B	C	D	E	F
P3	19	GND	GND	GND	GND	GND	GND	GND
	18	GND	+3.3V	+5V	+12V	-12V		GND
	17	GND	IPMB_PWR	GND	GND	GND	GND	GND
	16	GND						GND
	15	GND	+12V	+12V	+12V	+12V	+12V	GND
	14	GND	INH#1	INH#2	INH#3	INH#4		GND
	13	GND	FAL1N	FAL2N	FAL3N	FAL4N		GND
	12	GND		+12V		+12V		GND
	11	GND						GND
	10	GND	+12V		+12V		+12V	GND
	9	GND						GND
	8	GND	IPMB_PWR	IPMB_PWR				GND
	7	GND	B_IPMB_SCL	B_IPMB_SD				GND
	6	GND	IPMB_PWR	IPMB_PWR	A_SMB_ALERT	IPMB_PWR	IPMB_PWR	GND
	5	GND	A_IPMB_SCL	A_IPMB_SD	IPMB_PWR	C_IPMB_SEL	C_IPMB_SDA	GND
	4	GND	GND	GND	GND	GND	GND	GND
	3	GND			GND			GND
	2	GND	TACH3	TACH4	GND	PWM3	PWM4	GND
	1	GND	TACH1	TACH2	GND	PWM1	PWM2	GND

Table 22 : Pinout for Alarm Slot P1 and P2

		Column						
	Row	Z	A	B	C	D	E	F
P2	22					GA1	GA0	GND
	21		LPa_DA+	LPa_DA-	GND			GND
	20		LPa_DB+	LPa_DB-	GND		FAL_OUT1	GND
	19		LPb_DA+	LPb_DA-	GND		DEG_OUT1	GND
	18		LPb_DB+	LPb_DB-	GND			GND
	17		5V(a)	5V(b)	GND			GND
	16						DEG1N	GND
	15						FAL1N	GND
	14						INH#1	GND
	13						DEG2N	GND
	12						FAL2N	GND
	11						INH#2	GND
	10						DEG3N	GND
	9						FAL3N	GND
	8						INH#3	GND
	7						DEG4N	GND
	6						FAL4N	GND
	5						INH#4	GND
	4							GND
	3							GND
	2							GND
	1							GND
P1	25							GND
	24							GND
	23							GND
	22							GND
	21		B_PRSTN					GND
	20		A_PRSTN				INH#	GND
	19		B_ENUMN			3.3V(a)		GND
	18		A_ENUMN					GND
	17					3.3V(b)		GND
	16							GND
	15		-12V(a)			GND	PEM2_PR	GND
	14		KEY					
	13							
	12							
	11						PEM1_PR	GND
	10		IPMB_PWR	C_IPMB_SCL	C_IPMB_SDA			GND
	9		IPMB_PWR	B_IPMB_SCL	B_IPMB_SDA	B_SMB_ALERT#	PEM2_INH	GND
	8		IPMB_PWR	A_IPMB_SCL	A_IPMB_SDA	A_SMB_ALERT#	PEM1_INH	GND
	7							GND
	6						PEM2INOK	GND
	5		TACH4	PWM4	TEMP4	TEMP/4	PEM1INOK	GND
	4		TACH3	PWM3	TEMP3	TEMP/3		GND
	3		TACH2	PWM2	TEMP2	TEMP/2	PEM2OUTOK	GND
	2		TACH1	PWM1	TEMP1	TEMP/1	PEM1OUTOK	GND
	1		+12V(a)	+12V(a)	+12V(b)	+12V(b)	-12V(b)	GND

Short Pins Medium Pins Long Pins

4.5.1 Configuring for use without an Alarm Card

When an alarm card is not installed in slot 17, jumper shunts must be loaded in headers JP4, JP5 and JP6. If an alarm card is installed, make sure all jumpers are removed.

The factory default configuration has these jumpers loaded.

Table 23 displays the allocation of signals on JP4, JP5 and JP6. The signals next to 'SBC' are the signals that will be connected to if the shunt is installed. Note that shunts are only required if the corresponding power supply connector is present.

Table 23: Power Signal Strapping

Pins	JP4	JP5	JP6	Supply
1,2	INH1#	FAL1N	DEG1N	J1
3,4	INH2#	FAL2N	DEG2N	J2
5,6	INH3#	FAL3N	DEG3N	J3
7,8	INH4#	FAL4N	DEG4N	J8
SBC	INH#	FALN	DEGN	

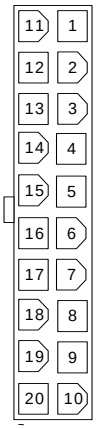
4.6 Miscellaneous connectors

4.6.1 ATX power connector ($)

As an option, a 20-pin ATX connector can be populated. This connector (JP10) can be utilized to power the backplane in a lab environment or to power external devices. Current to each of the pins is limited to 9 amps. Table 24 displays the connector footprint and pinout.

Table 24: ATX Connector Pinout and Footprint

Description	Pin	Pin	Description
+3.3V	**11**	**1**	+3.3V
-12V	**12**	**2**	+3.3V
GND	**13**	**3**	GND
INH#	**14**	**4**	+5V
GND	**15**	**5**	GND
GND	**16**	**6**	+5V
GND	**17**	**7**	GND
-5V	**18**	**8**	FALN
+5V	**19**	**9**	+5V
+5V	**20**	**10**	+12V



** Pin 1 (1) Connects +3.3V on an ATX power supply to the 3.3V plane of the backplane.

** Pin 8 (1) Connects PW_OK on an ATX power supply to the FAL# signal on the CompactPCI® Host slot.

** Pin 9 (1) Connects 5VSB on an ATX power supply to the DEG# signal on the CompactPCI® Host slot.

** Pin 14 (1) Connects PS_ON on an ATX power supply to the INHIBIT signal on the Control header.

** Pin 16 (1) Connects GND on an ATX power supply to the GND plane of the backplane.

** Pin 18 (1) Connects –5V on an ATX power supply to the 12V plane of the backplane (through a jumper).

** Pin 19 (1) Connects +5V on an ATX power supply to the 5V plane of the backplane.

** NOTE: These signals are not standard ATX signals. INH#, DEG#, and FAL# are connected directly to the CompactPCI® power supply connectors. Please see the CompactPCI® specification for a description of these signals.

4.7 Regulatory and safety

The PS4900/05 has been designed to comply with the following standards:

- EN 60950
- UL 1950

A clearance of 2.5mm has been provided between AC voltages and chassis ground on all external layers. A clearance of 5mm has been provided between AC and secondary voltages on all internal layers. A clearance of 0.4mm has been provided between primary and secondary voltages on all internal layers.

5 Appendix A

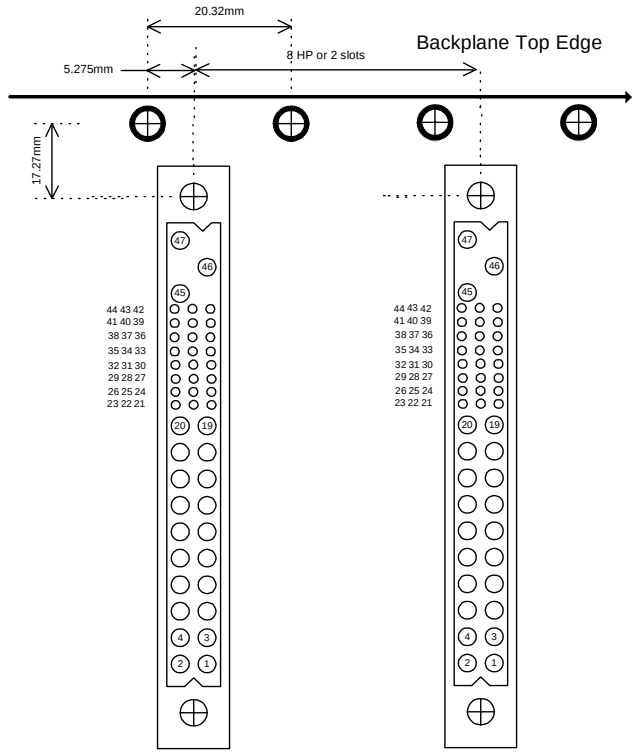
5.1 47 Pin Positronic

The large contacts (size 16) in positions 45, 46 and 47 have a current capacity of 40A each, derated to 23A for a 30ºC temperature rise. The large contacts (size 16) in positions 1-20 have a current capacity of 28A each, derated to 16.5A for a 30ºC temperature rise. The small contacts (size 22) have a capacity of 3A nominal each. **Table 25** displays the pinout, outline and location of the 47-pin power supply connectors.

Table 25: Pinout, outline and location of the 47-pin Positronic Connectors

(as viewed from connector side of the backplane or front of rack)

Pin(s)	Signal
1-4	+5V
5-12	GND
13-18	+3.3V
19	GND
20	+12V
21	-12V
22	GND
23	N/C
24	GND
25	GA0
26	N/C
27	GND
28	GA1
29	N/C
30	+5V_SENSE
31	GA2
32	N/C
33	+3V_SENSE
34	GND
35	+5V _SHARE
36	+12V_SENSE
37	IPMB_SCL
38	DEG#
39	INH#
40	IPMB_SDA
41	+3V _SHARE
42	FAL#
43	IPMB_PWR
44	+12V_ SHARE
45	CHASSIS_GND
46	AC_NEUT/DC
47	AC_HOT/DC-



Backplane Power Connector Location as viewed from the front of the cardcage

The mechanical location of the power supply connectors conforms to the PICMG® 2.11 R1.0, Power Interface Specification.

5.2 Backplane connectors

Table 26 displays all of the connectors utilized on the backplanes.

Table 26: Connectors used on the PS4900/05 backplanes

Description	Reference	Vendor	Connector P/N	Rating	Mating Connector P/N
47-pin pressfit	J1, J2, J3, J8	Positronic	PCIH47F9300A1	94V-0	
2x3 Mate-N-Lok	J12	AMP	350732-1	94V-0	350715-1
PEM connector	J17, J22	Elcon	278-0962-00200A		
I/O connector	P1	AMP	102699-9	94V-0	87977-8
20-pin ATX style	J10	Molex	44472-2055	94V-0	39-01-2205
		AMP	2-794666-0 (LC)	94V-0	2-794657-0 (LC)
Fan connector	J51, J52, J53	Molex	43879-0023		39-01-2600
1x3 Mate-N-Lok	J14 – J16	AMP	350790-1		350766-1
SMB Connector	J4, J5	Molex	53398-0590	94V-0	87439-0500
		Molex (RA)	53261-0590	94V-0	87439-0500
1x2 Locking header	J100	Molex	22-11-2022	94V-0	50-57-9502
		AMP	641126-2	94V-0	
A25-S-HS	Px1	Erni	923190	94V-0	
		EPT	243-11322-15		
	x=1..16	AMP	352332-1	94V-0	
A25-LT	Px4	Erni	923347	94V-0	
(PS4900)	x=1, 8, 9, 16	EPT	243-11737-15		
(PS4905)	x=1..16	AMP	1-345237-1		
A25-TEL	Px4	Erni	923160	94V-0	
(PS4900 only)		EPT	243-11323-15		
	x=2..7, 10..15	AMP	352352-1	94V-0	
AB19-LT	Px3	Erni	923694	94V-0	
		EPT	243-63701-15		
	x=1..16	AMP	N/A		
B19-S	rP173	Erni	103670	94V-0	
		EPT	243-23320-15		
		AMP	352033-1	94V-0	
B22-S	Px2	Erni	914796	94V-0	
		EPT	243-22320-15		
	x=1..16	AMP	188835-1	94V-0	
B22-TEL	Px5	Erni	923339	94V-0	
(PS4900 only)		EPT	243-22362-15		
	x=1..16	AMP	1-345047-1		
B22-LT	Px5	Erni	923345	94V-0	
(PS4905 only)		EPT	243-22713-15		

Description	Reference	Vendor	Connector P / N	Rating	Mating Connector P / N
	x=1..16	AMP	1-345236-1		
A25 Shroud	SHx4	Erni	54795	94V-0	
(PS4900)	x=1, 8, 9, 16	EPT	243-5525-1		
(PS4905)	x=1..16	AMP	646478-3		
AB19 Shroud	SHx3	Erni	114488	94V-0	
		EPT	243-5719-1		
	x=1..16	AMP	646483-5		
AB22 Shroud	SHx5	Erni	114426	94V-0	
		EPT	243-5722-1		
	x=1..16	AMP	646484-5		
SIM P1	P171	Erni	923772	94V-0	
SIM P2	P172	Erni	923345	94V-0	
SIM P1 Shroud	SH171	Erni	054795	94V-0	
SIM P2 Shroud	SH172	Erni	114426	94V-0	

S - Short Tail LT - Long Tail HS - Hot Swap LC – Low Current

6 Appendix B

6.1 CompactPCI® Host slot P1 and P2 pinout

Table 27: Host Slot P1 & P2 Pinout

		Column						
	Row	**Z**	**A**	**B**	**C**	**D**	**E**	**F**
P2	22	GND	GA4	GA3	GA2	GA1	GA0	GND
	21	GND	CLK6	GND	RSV	ST[1]	ST[0]	GND
	20	GND	CLK5	GND	RSV	GND	RSV	GND
	19	GND	GND	GND	SMB_SDA	SMB_SCL	SMB_ALERT#	GND
	18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
	17	GND	BRSVP2A17	GND	PRST#	REQ6#	GNT6#	GND
	16	GND	BRSVP2A16	BRSVP2B16	DEG# (1)	GND	BRSVP2E16	GND
	15	GND	BRSVP2A15	GND	FAL# (1)	REQ5#	GNT5#	GND
	14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
	13	GND	AD[38]	GND	VIO	AD[37]	AD[36]	GND
	12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
	11	GND	AD[45]	GND	VIO	AD[44]	AD[43]	GND
	10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
	9	GND	AD[52]	GND	VIO	AD[51]	AD[50]	GND
	8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
	7	GND	AD[59]	GND	VIO	AD[58]	AD[57]	GND
	6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
	5	GND	C/BE[5]#	GND	VIO	C/BE[4]#	PAR64	GND
	4	GND	VIO	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
	3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
	2	GND	CLK2	CLK3	GND (SYSEN#)	GNT2#	REQ2#	GND
	1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
P1	25	GND	+5V	REQ64#	ENUM#	+3.3V	+5V	GND
	24	GND	AD[1]	+5V	VIO	AD[0]	ACK64#	GND
	23	GND	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND
	22	GND	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
	21	GND	+3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
	20	GND	AD[12]	GND	VIO	AD[11]	AD[10]	GND
	19	GND	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
	18	GND	SERR#	GND	+3.3V	PAR	C/BE[1]#	GND
	17	GND	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
	16	GND	DEVSEL#	GND	VIO	STOP#	LOCK#	GND
	15	GND	+3.3V	FRAME#	IRDY#	GND	TRDY#	GND
	14							
	13				KEY			
	12							
	11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
	10	GND	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
	9	GND	C/BE[3]#	GND	AD[23]	GND	AD[22]	GND
	8	GND	AD[26]	GND	VIO	AD[25]	AD[24]	GND
	7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
	6	GND	REQ0#	PCI_PRESENT#	+3.3V	CLK0	AD[31]	GND
	5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0#	GND
	4	GND	IPMB_PWR	HEALTHY#	VIO	INTP	INTS	GND
	3	GND	INTA#	INTB#	INTC#	+5V	INTD#	GND
	2	GND	TCK	+5V	TMS	N/C	N/C	GND
	1	GND	+5V	-12V	TRST#	+12V	+5V	GND

Short Pins Medium Pins Long Pins

6.2 CompactPCI® Peripheral slot P1 and P2 pinout

Table 28: Peripheral Slot P1 & P2 Pinout

	Row	Column Z	A	B	C	D	E	F
P2	22	GND	GA4	GA3	GA2	GA1	GA0	GND
	21	GND	RSV	RSV	RSV	RSV	RSV	GND
	20	GND	RSV	RSV	RSV	GND	RSV	GND
	19	GND	RSV	RSV	RSV	RSV	RSV	GND
	18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
	17	GND	BRSVP2A17	GND	RSV	RSV	RSV	GND
	16	GND	BRSVP2A16	BRSVP2B16	RSV	GND	BRSVP2E16	GND
	15	GND	BRSVP2A15	GND	RSV	RSV	RSV	GND
	14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
	13	GND	AD[38]	GND	VIO	AD[37]	AD[36]	GND
	12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
	11	GND	AD[45]	GND	VIO	AD[44]	AD[43]	GND
	10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
	9	GND	AD[52]	GND	VIO	AD[51]	AD[50]	GND
	8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
	7	GND	AD[59]	GND	VIO	AD[58]	AD[57]	GND
	6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
	5	GND	C/BE[5]#	GND	VIO	C/BE[4]#	PAR64	GND
	4	GND	VIO	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
	3	GND	RSV	GND	RSV	RSV	RSV	GND
	2	GND	RSV	RSV	N/C	RSV	RSV	GND
	1	GND	RSV	GND	RSV	RSV	RSV	GND
P1	25	GND	+5V	REQ64#	ENUM#	+3.3V	+5V	GND
	24	GND	AD[1]	+5V	VIO	AD[0]	ACK64#	GND
	23	GND	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND
	22	GND	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
	21	GND	+3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
	20	GND	AD[12]	GND	VIO	AD[11]	AD[10]	GND
	19	GND	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
	18	GND	SERR#	GND	+3.3V	PAR	C/BE[1]#	GND
	17	GND	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
	16	GND	DEVSEL#	GND	VIO	STOP#	LOCK#	GND
	15	GND	+3.3V	FRAME#	IRDY#	GND	TRDY#	GND
	14	KEY						
	13							
	12							
	11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
	10	GND	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
	9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
	8	GND	AD[26]	GND	VIO	AD[25]	AD[24]	GND
	7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
	6	GND	REQ#	PCI_PRESENT#	+3.3V	CLK	AD[31]	GND
	5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
	4	GND	IPMB_PWR	HEALTHY#	VIO	INTP	INTS	GND
	3	GND	INTA#	INTB#	INTC#	+5V	INTD#	GND
	2	GND	TCK	+5V	TMS	N/C	N/C	GND
	1	GND	+5V	-12V	TRST#	+12V	+5V	GND

Short Pins Medium Pins Long Pins

6.3 CompactPCI® H.110 P4 pinout (PS4900 only)

Table 29: H.110 P4 Pinout

Row		Column						
		Z	**A**	**B**	**C**	**D**	**E**	**F**
P4	25	GND	SGA4	SGA3	SGA2	SGA1	SGA0	GND
	24	GND	GA4	GA3	GA2	GA1	GA0	GND
	23	GND	+12V	CT_RESET# (4)	CT_EN#	-12V	CT_MC	GND
	22	GND	PFS0# (3)	N/C	N/C	N/C	RSVD	GND
	21	GND	-SELVbat	PFS1# (3)	N/C	N/C	SELVbatRtn	GND
	20	GND	NP (1)	NP (1)	NP (1)	NP (1)	NP (1)	GND
	19	GND	NP (1)	NP (1)	NP (1)	NP (1)	NP (1)	GND
	18	GND	VRG (3)	NP (1)	NP (1)	NP (1)	VRGRtn	GND
	17	GND	NP (1)	NP (1)	NP (1)	NP (1)	NP (1)	GND
	16	GND	NP (1)	NP (1)	NP (1)	NP (1)	NP (1)	GND
	15	GND	-Vbat	NP (1)	NP (1)	NP (1)	VbatRtn	GND
	14		KEY					
	13							
	12							
	11	GND	CT_D29	CT_D30	CT_D31	V(I/O)	CT_FRAME_A#	GND
	10	GND	CT_D27	+3.3V	CT_D28	+5V	CT_FRAME_B#	GND
	9	GND	CT_D24	CT_D25	CT_D26	GND	FR_COMP#	GND
	8	GND	CT_D21	CT_D22	CT_D23	+5V	CT_C8_A	GND
	7	GND	CT_D19	+5V	CT_D20	GND	CT_C8_B	GND
	6	GND	CT_D16	CT_D17	CT_D18	GND	CT_NETREF_1	GND
	5	GND	CT_D13	CT_D14	CT_D15	+3.3V	CT_NETREF_2	GND
	4	GND	CT_D11	+5V	CT_D12	+3.3V	SCLK	GND
	3	GND	CT_D8	CT_D9	CT_D10	GND	SCLK-D	GND
	2	GND	CT_D4	CT_D5	CT_D6	CT_D7	GND	GND
	1	GND	CT_D0	+3.3V	CT_D1	CT_D2	CT_D3	GND

Short Pins Medium Pins Long Pins

6.4 CompactPCI® 2.16 Standard Fabric Slot connectors

Table 30: Standard Fabric P3 And P5

Row		Column						
		Z	**A**	**B**	**C**	**D**	**E**	**F**
P5	22	GND	N/C	N/C	GND	N/C	N/C	GND
	21	GND	N/C	N/C	GND	N/C	N/C	GND
	20	GND	N/C	N/C	GND	N/C	N/C	GND
	19	GND	N/C	N/C	GND	N/C	N/C	GND
	18	GND	N/C	N/C	GND	N/C	N/C	GND
	17	GND	N/C	N/C	GND	N/C	N/C	GND
	16	GND	N/C	N/C	GND	N/C	N/C	GND
	15	GND	N/C	N/C	GND	N/C	N/C	GND
	14	GND	N/C	N/C	GND	N/C	N/C	GND
	13	GND	N/C	N/C	GND	N/C	N/C	GND
	12	GND	LP14_DA+	LP14_DA-	GND	LP14_DC+	LP14_DC-	GND
	11	GND	LP14_DB+	LP14_DB-	GND	LP14_DD+	LP14_DD-	GND
	10	GND	LP13_DA+	LP13_DA-	GND	LP13_DC+	LP13_DC-	GND
	9	GND	LP13_DB+	LP13_DB-	GND	LP13_DD+	LP13_DD-	GND
	8	GND	LP12_DA+	LP12_DA-	GND	LP12_DC+	LP12_DC-	GND
	7	GND	LP12_DB+	LP12_DB-	GND	LP12_DD+	LP12_DD-	GND
	6	GND	LP11_DA+	LP11_DA-	GND	LP11_DC+	LP11_DC-	GND
	5	GND	LP11_DB+	LP11_DB-	GND	LP11_DD+	LP11_DD-	GND
	4	GND	LP10_DA+	LP10_DA-	GND	LP10_DC+	LP10_DC-	GND
	3	GND	LP10_DB+	LP10_DB-	GND	LP10_DD+	LP10_DD-	GND
	2	GND	LP9_DA+	LP9_DA-	GND	LP9_DC+	LP9_DC-	GND
	1	GND	LP9_DB+	LP9_DB-	GND	LP9_DD+	LP9_DD-	GND
P3	19	GND	SGA4	SGA3	SGA2	SGA1	SGA0	GND
	18	GND	LPf_DA+	LPf_DA-	GND	LPf_DC+	LPf_DC-	GND
	17	GND	LPf_DB+	LPf_DB-	GND	LPf_DD+	LPf_DD-	GND
	16	GND	LP8_DA+	LP8_DA-	GND	LP8_DC+	LP8_DC-	GND
	15	GND	LP8_DB+	LP8_DB-	GND	LP8_DD+	LP8_DD-	GND
	14	GND	LP7_DA+	LP7_DA-	GND	LP7_DC+	LP7_DC-	GND
	13	GND	LP7_DB+	LP7_DB-	GND	LP7_DD+	LP7_DD-	GND
	12	GND	LP6_DA+	LP6_DA-	GND	LP6_DC+	LP6_DC-	GND
	11	GND	LP6_DB+	LP6_DB-	GND	LP6_DD+	LP6_DD-	GND
	10	GND	LP5_DA+	LP5_DA-	GND	LP5_DC+	LP5_DC-	GND
	9	GND	LP5_DB+	LP5_DB-	GND	LP5_DD+	LP5_DD-	GND
	8	GND	LP4_DA+	LP4_DA-	GND	LP4_DC+	LP4_DC-	GND
	7	GND	LP4_DB+	LP4_DB-	GND	LP4_DD+	LP4_DD-	GND
	6	GND	LP3_DA+	LP3_DA-	GND	LP3_DC+	LP3_DC-	GND
	5	GND	LP3_DB+	LP3_DB-	GND	LP3_DD+	LP3_DD-	GND
	4	GND	LP2_DA+	LP2_DA-	GND	LP2_DC+	LP2_DC-	GND
	3	GND	LP2_DB+	LP2_DB-	GND	LP2_DD+	LP2_DD-	GND
	2	GND	LP1_DA+	LP1_DA-	GND	LP1_DC+	LP1_DC-	GND
	1	GND	LP1_DB+	LP1_DB-	GND	LP1_DD+	LP1_DD-	GND

7 Glossary

The following list will provide some insight into terms used throughout this document.

3U

A half height CompactPCI® slot or card.

4 HP

The width of a typical single wide CompactPCI® slot. The distance between adjacent 4 HP slots is exactly 0.800″.

6U

A full height CompactPCI® slot or card.

8 HP

The width of a double wide CompactPCI® slot. This type of slot is commonly used for power supplies and SBC modules.

HP

This terminology refers to a unit of width commonly used within the CompactPCI® mechanical specifications. One HP is 0.200″.

J1-J5

See P1-P5.

P1-P5

The CompactPCI® specification uses the terminology P1, P2, P3, P4, P5, J1, J2, J3, J4, and J5 to refer to specific connector locations within a backplane slot and on a plug in card. The prefix P denotes a connector on the backplane the prefix J denotes the mating connector on the CompactPCI® cards. The connectors are numbered from P1 to P5 starting at the bottom of a 6U slot.

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